In the specification:

Please amend paragraph [0005] on page 2 as follows:

[0005] A particular disadvantage about known concepts for fabricating fin filed-effect transistors ~~isthat~~ is that, relative to channel length, the fin field-effect transistors can only be arranged in a relatively low packing density compared with conventional planar or vertical field-effect transistor structures. This is disadvantageous, in particular, in an application of the fin field-effect transistors as selection transistors of capacitive memory cells.

Please amend paragraph [0024] on page 6 as follows:

[0024] Figure[[s]] ~~2a and 2b~~ 2 shows a cross section through three original fins 2' arranged next to one another for fin field-effect transistors fabricated in accordance with an embodiment of the present invention, after the application of an isolating dielectric 5. In this case, firstly original fins 2' arranged next to one another and running parallel, are formed on a semiconductor substrate 1 by a first lithography step. In the present exemplary embodiment, the material of the original fins 2' and that of the semiconductor substrate 1 is monocrystalline silicon.